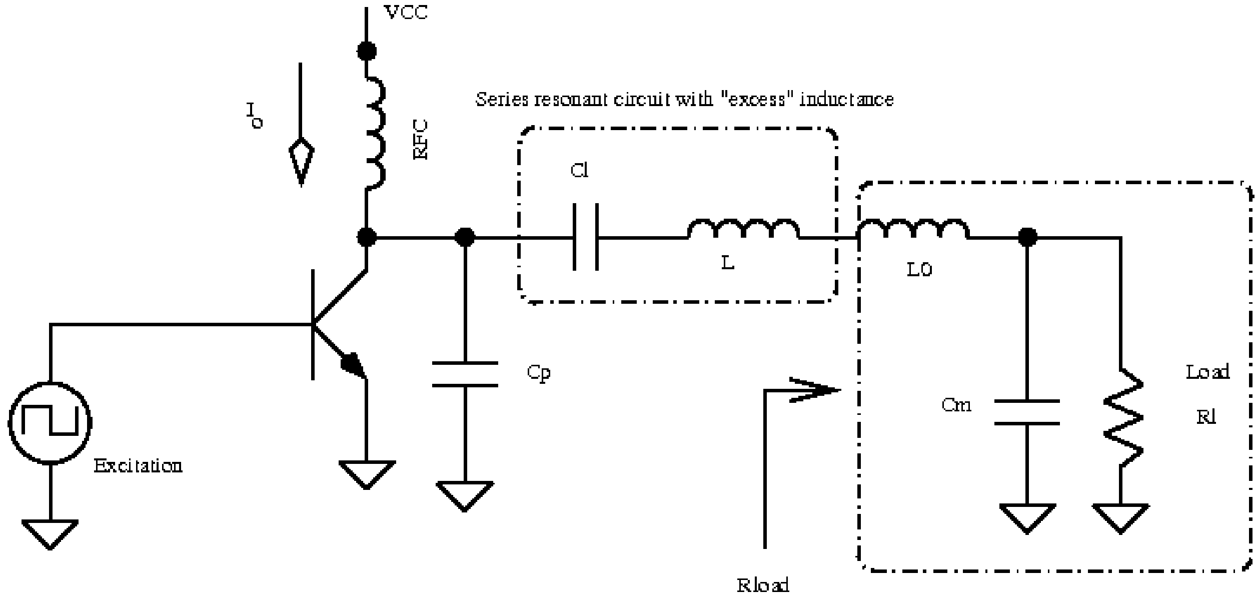
Class-E design process

This design process is based on the assumption of a "perfect" transistor switch and an output network Q-factor greater than about 5-7 (10% or so error) and a perfect inductive choke between the drain and power supply. Output circuit blocks all harmonics allowing only fundamental frequency power to load. This is not completely valid for low Q As output Q factor rises to 10 or more, the assumption of fundamental signal transmission to the load with negligible harmonic content becomes more valid.



Component	Name/Function	Notes
RFC	Bias choke	Impedance at least 10-15 times R_{load}
C_p	Drain shunt capacitance	Combination of intrinsic drain source capacitance and externally applied capacitance
C_l	Series capacitance	Needed to achieve Q-factor
L	Series inductor	Combination of "series resonant" LC network inductance L_{res} plus excess inductance L_{exc} to achieve proper fundamental drain current/voltage phasing. $L=L_{res}+L_{exc}$
L_0	Matching inductor	Part of L-match to 50 ohm load. This is absorbed into L.
C_m	Matching capacitor	Part of L-match to 50 ohms
R_l	Load resistor	50 ohms (usually, but not necessarily).
R_{load}	Resistive part of load seen by switch at fundamental frequency	This is transformed by the L-match network to R_l (50 ohms, etc.)

For the design, we need to specify:

1. Output power P_{load}
2. The load impedance R_l (usually 50Ω).
3. Supply voltage V_{cc}. (Note: this needs to be based on max transistor breakdown voltage, which should be more than 3.6 times the supply voltage.)
4. Operating center frequency $\omega = 2\pi \cdot f$.
5. Desired output circuit Q (Determines bandwidth, choose > 5 or so, otherwise component values shift as a result of the simplifying assumptions used in the analysis. Q=10 or more gives very little error).

- Step 1: If switching device shunt capacitance is known, specify the desired output power P_{load} and the DC supply voltage V_{cc}. This yields a relationship between I_0 and the load resistance from

$$P_{load} = \frac{8 \cdot V_{cc}^2}{(\pi^2 + 4)R_{load}} = V_{cc} I_0 .$$

- From the expected supply voltage and currents needed to provide the desired power, the drain-source shunt capacitance is yielded by

$$I_0 = \omega \pi \cdot C_P V_{cc} .$$

- Compute the required "excess inductance" L_{exc}:

$$L_{exc} = \frac{1.153 \cdot R_{load}}{\omega}$$

- Compute the resonant inductance L_{res} and the series capacitance based on chosen Q factor and resonant frequency ω:

$$C_l = \frac{1}{Q \cdot R_{load} \cdot \omega}$$

$$L_{res} = \frac{Q \cdot R_{load}}{\omega} .$$

- Compute the L-match parallel capacitance based on the values for R_l and R_{load}:

$$C_m = \frac{1}{\omega \cdot R_l} \sqrt{\frac{R_l}{R_{load}} - 1} .$$

- Calculate L-match series inductance:

$$L_0 = C_m \cdot R_l \cdot R_{load} .$$

We now have the full design. Looking at a specific example, let us choose a set of specifications.

1. V_{cc}=12V
2. P_{load}=5W
3. Q=10
4. $\omega = 2\pi \cdot 6.9 \times 10^6$ rad/sec

Following the design procedure, we compute

- $R_{load} = \frac{8 \cdot V_{cc}^2}{(\pi^2 + 4)P_l} = \frac{(8)(12)(12)}{(13.869)(5)} = 16.6\Omega$
- $I_0 = \frac{P_{load}}{V_{cc}} = \frac{5}{12} = 0.4167A$

The needed shunt drain-source capacitance.

- $C_P = \frac{I_0}{\omega \cdot \pi \cdot V_{cc}} = \frac{0.4167}{(6.283)(6.9x10^6)(3.1415)(12)} = 255pF$

The excess inductance needed to have Class-E operation.

- $L_{exc} = \dfrac{1.153 \cdot R_{load}}{\omega} = \dfrac{(1.153)(16.6)}{(6.283)(6.9x10^6)} = 441nH$

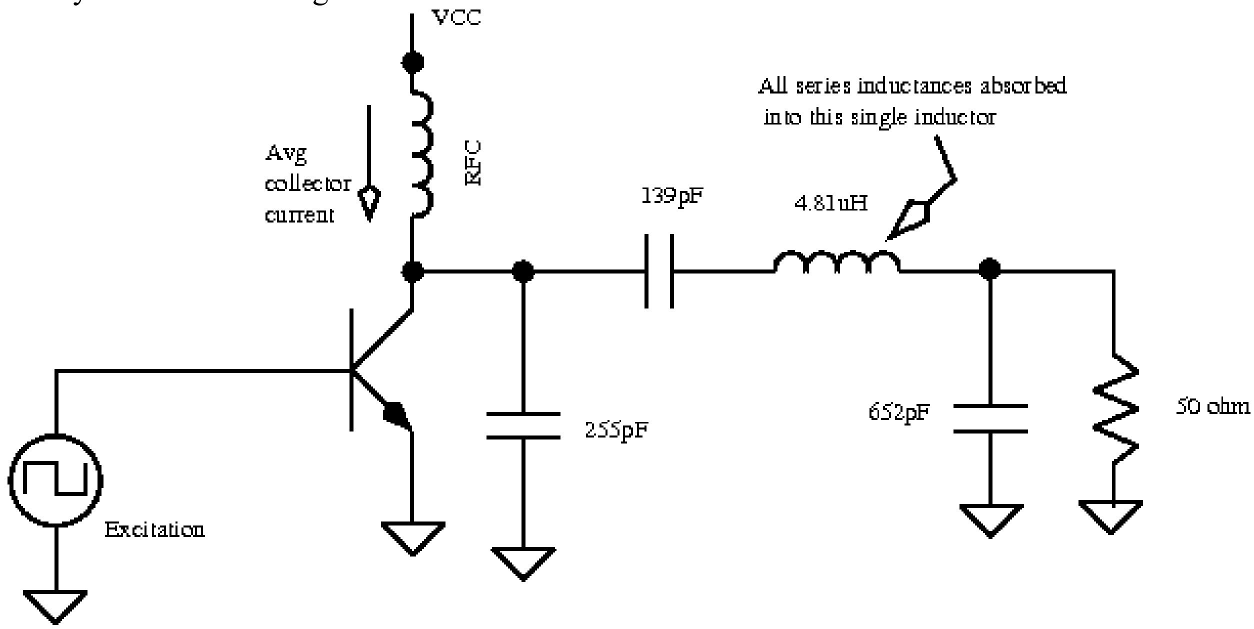
The resonant part at 6.9MHz with a Q of 10.

- $C_l = \dfrac{1}{(10)(16.67)(6.283)(6.9x10^6)} = 139pF$
- $L_{res} = \dfrac{Q \cdot R_{load}}{\omega} = \dfrac{(10)(16.67)}{(6.28)(6.9x10^6)} = 3.829uH$

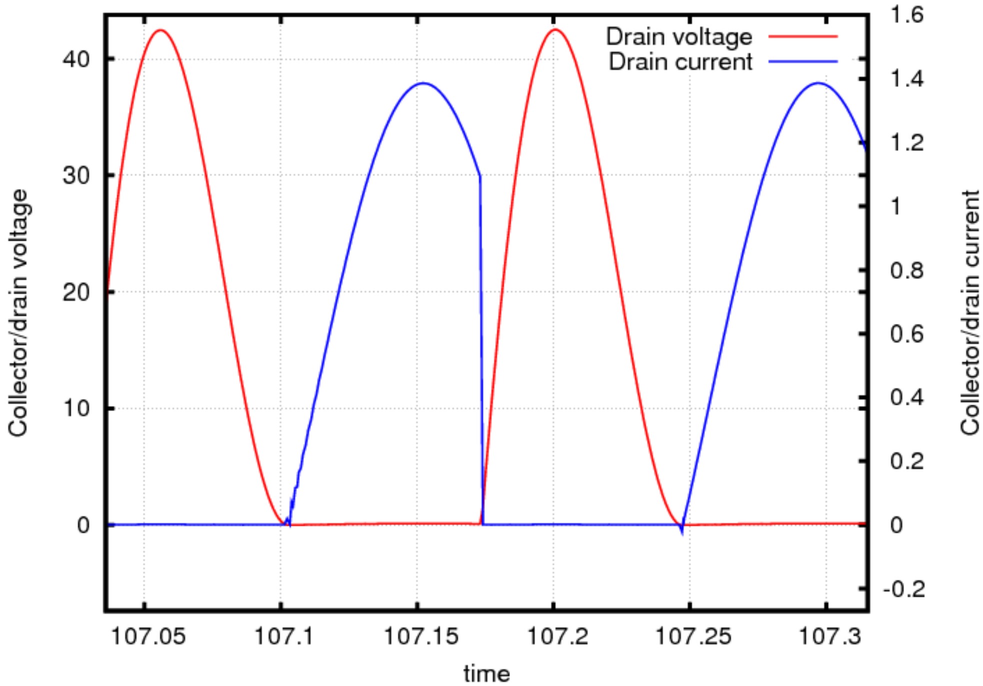
L-match to 50 ohm load.

- $C_m = \dfrac{1}{(6.283)(6.9x10^6)(50)}\sqrt{\dfrac{50}{16.67} - 1} = 652pF$
- $L_0 = (6.52x10^{-10})(50)(16.67) = 544nH$

This yields the following circuit.



This circuit yields the drain waveforms that clearly exhibit class e characteristics.



Drain voltage
Drain current
Collector/drain voltage
Collector/drain current
time
40
30
20
10
0
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
107.05
107.1
107.15
107.2
107.25
107.3